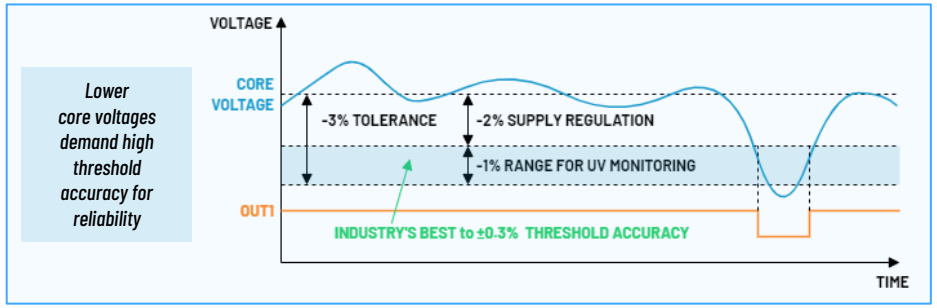
Supervisory Devices Complementary Parts Guide for Altera FPGAs

Modern FPGA designs leverage advance fabrication techniques, enabling smaller process geometries and lower core voltages. This trend, however, necessitate the use of multiple voltage rails to accommodate legacy I/O standards. To guarantee system stability and prevent unexpected behavior, each of these voltage rails requires dedicated supervision.

Analog Devices provides a comprehensive portfolio of voltage monitoring solutions, encompassing a wide range; from basic single-channel to feature-rich multi-voltage supervisors boasting industry-leading accuracy (up to ±0.3% across temperatures).

The core and I/O voltage requirements for various Altera® FPGA families are presented in a clear and easy-to-reference table. Core voltage ranges typically span from 0.70 V to 1.2 V, while I/O voltage levels can vary between 1 V and 3.3 V.



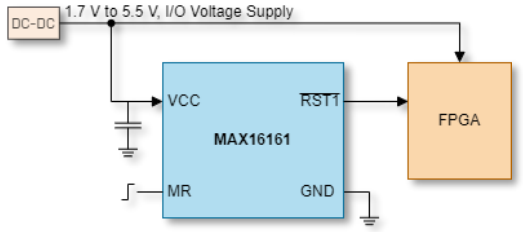
Multi-voltage Supervisors with Altera FPGAs

Altera FPGAs

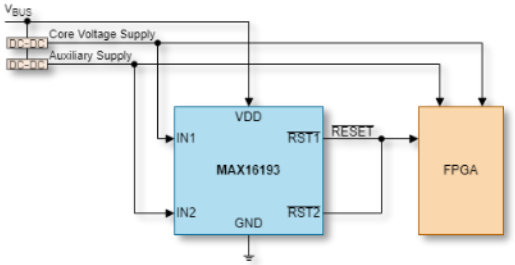
Altera FPGA Family	Core Voltage (V)	I/O Voltage (V)
Agilex 7 F	0.70 - 0.90	1.2, 1.5
Agilex 7 I	0.70 - 0.90	1.2, 1.5
Stratix 10	0.8 - 0.94	1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 3, 3.3
Stratix V	0.85, 0.9	1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 3.0
Stratix IV	0.9	1.2, 1.5, 1.8, 2.5, 3.0
Arria 10	0.9, 0.95	1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 3.0
Arria V GX	1.1, 1.15	1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 3.0, 3.3
Arria V GZ	0.85	1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 3.0
Cyclone 10 GX	0.9	1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 3.0
Cyclone 10 LP	1.0, 1.2	1.2, 1.5, 1.8, 2.5, 3, 3.3
Cyclone V	1.1, 1.15	1.2, 1.25, 1.35, 1.5, 1.8, 2.5, 3.0, 3.3
Cyclone IV	1.0, 1.2	1.2, 1.5, 1.8, 2.5, 3, 3.3
MAX 10	1.2 or 3.0, 3.3	1.0, 1.2, 1.35, 1.5, 1.8, 2.5, 3, 3.3

ADI Multi-voltage Supervisors

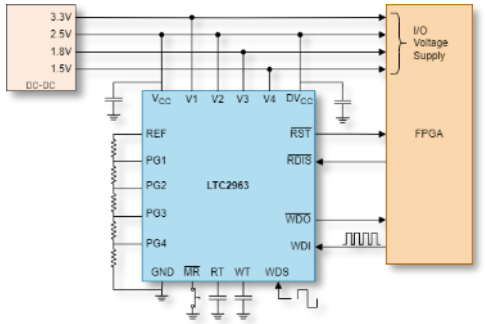
Number of Voltages Monitored	Part Number	Voltages Monitored (V)	Accuracy (%)
1	MAX16132	1.0 to 5.0	<1
1	MAX16161, MAX16162	1.7 to 4.85, 0.6 to 4.85	<1.5
2	MAX16193	0.6 to 0.9, 0.9 to 3.3	<0.3
3	MAX16134	5.0, 4.8, 4.5, 3.3, 3.0, 2.5, 1.8, 1.2, 1.16, 1.0	<1
4	LTC2962, LTC2963, LTC2964	5.0, 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, 0.5V	<0.5
4	MAX16135	5.0, 4.8, 4.5, 3.3, 3.0, 2.5, 2.3, 1.8, 1.5, 1.36, 1.22, 1.2, 1.16, 1.0	<1
4	MAX16060	3.3, 2.5, 1.8, 0.62 (adj)	<1
6	LTC2936	0.2 to 5.8 (Programmable)	<1



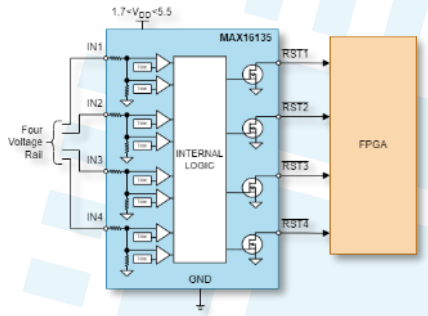
MAX16161: nanoPower Supply Supervisor with Glitch-Free Power-Up and Manual Reset



MAX16193: ±0.3% Accuracy Dual-Channel Window-Detector Supervisory Circuit



LTC2963: ±0.5% Quad Configurable Supervisor with Watchdog Timer



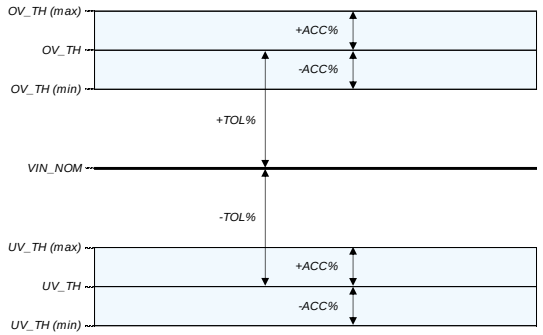
MAX16135: ±1% Low-Voltage, Quad-Voltage Window Supervisor

Window Voltage Supervisors

Window voltage supervisors are used to ensure FPGAs operate within a safe voltage specification range. They do this by having undervoltage (UV) and overvoltage (OV) thresholds and generating a reset output signal if it goes beyond the tolerance window to avoid system errors and prevent damage to your FPGAs and other processing devices. There are two main things to consider when choosing a window voltage supervisor: Tolerance and Threshold Accuracy.

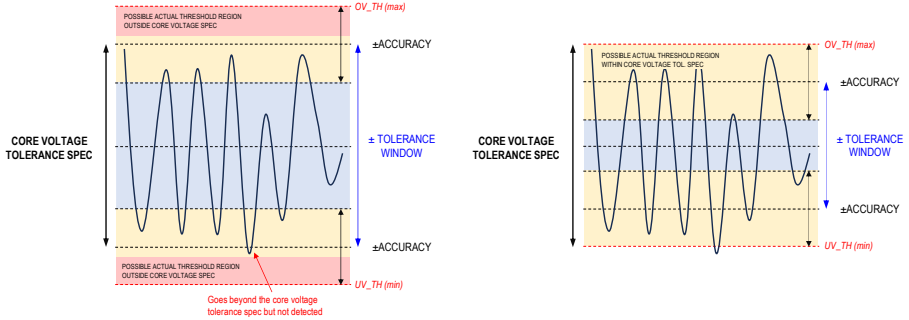
Tolerance is the range around the nominal monitored value which sets the overvoltage and undervoltage thresholds. While, Threshold Accuracy, typically expressed in percentage, is the degree of the conformance of the actual to the target reset thresholds.

Undervoltage and overvoltage threshold variation with Threshold Accuracy



Selecting the Right Tolerance Window

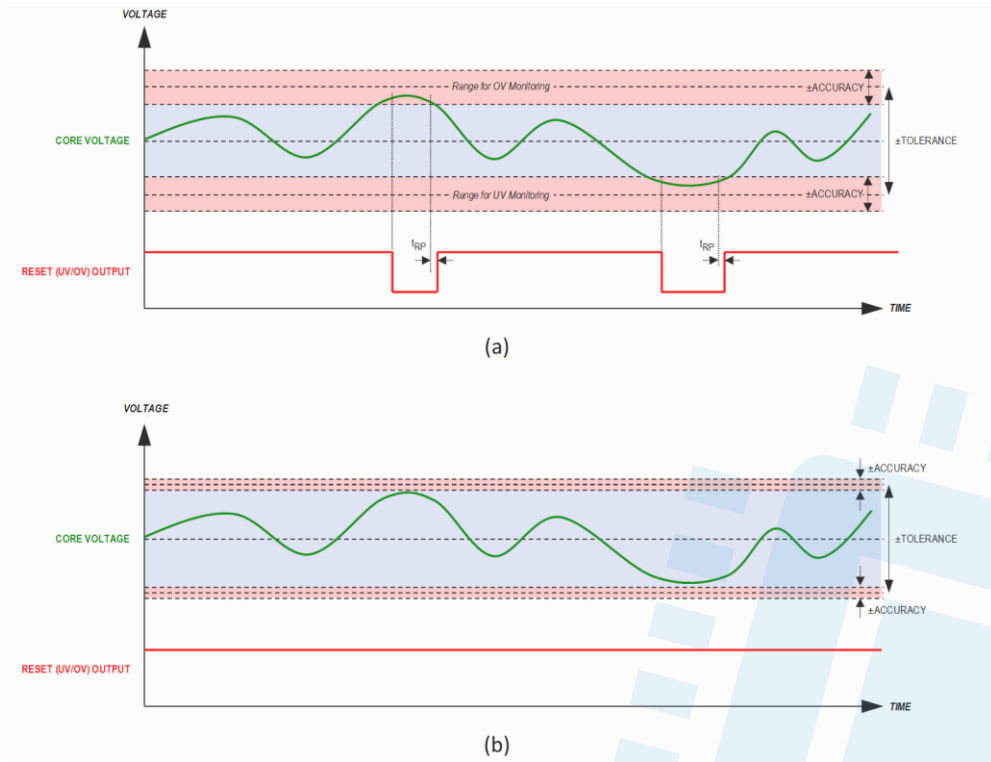
Choosing a window supervisor with the same tolerance as the core voltage requirement can lead to malfunctions due to threshold accuracy. Setting the same tolerance with the operating requirement of the FPGA can trigger a reset output near the maximum overvoltage threshold OV_TH (max) and minimum undervoltage threshold UV_TH (min). The figure below illustrates tolerance setting (a) same with core voltage tolerance vs. (b) within the core voltage tolerance.



Impact of Threshold Accuracy

Compare two window voltage supervisors with different threshold accuracy monitoring the same core voltage supply rail. The supervisor with higher threshold accuracy will deviate less from the threshold limits in comparison to voltage supervisors with lower accuracy.

Examining the figure below, window supervisors with lower accuracy (a) creates a narrow power supply window since the reset output signal can assert anywhere within the UV and OV monitoring range. In applications with unreliable power supply regulation, this could pose a more sensitive system prone to oscillation. On the other hand, supervisors with high threshold accuracy (b) expands this range to provide a wider safe operating range for your power supply which improves the systems overall performance.



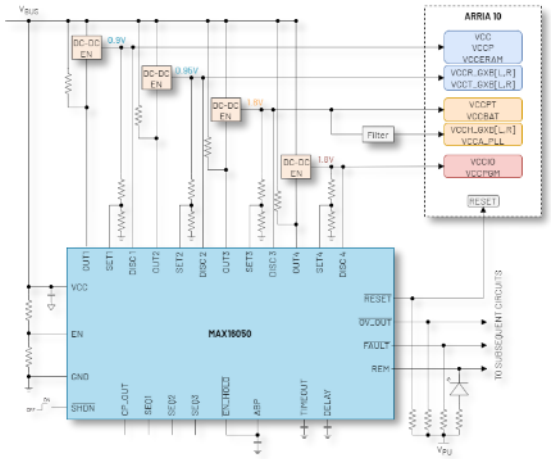
Power Supply Sequencing

Modern FPGAs utilize multiple voltage rails for optimal performance. Defined power-up and power-down sequencing requirement is crucial for FPGA reliability. Improper sequencing introduce glitches, logic errors, and even permanent damage to sensitive FPGA components.

Analog Devices offers a comprehensive range of supervisory/sequencing circuits specifically designed to address the challenges of FPGA power management. These devices orchestrate the power-up and power-down sequence of various voltage rails, guaranteeing that each rail reaches its designated voltage level within its required ramp time and order. This power management solution minimizes inrush current, prevents voltage undershoot/overshoot conditions, and ultimately safeguards the integrity of your FPGA design

ADI Supervisory and Sequencing Solutions

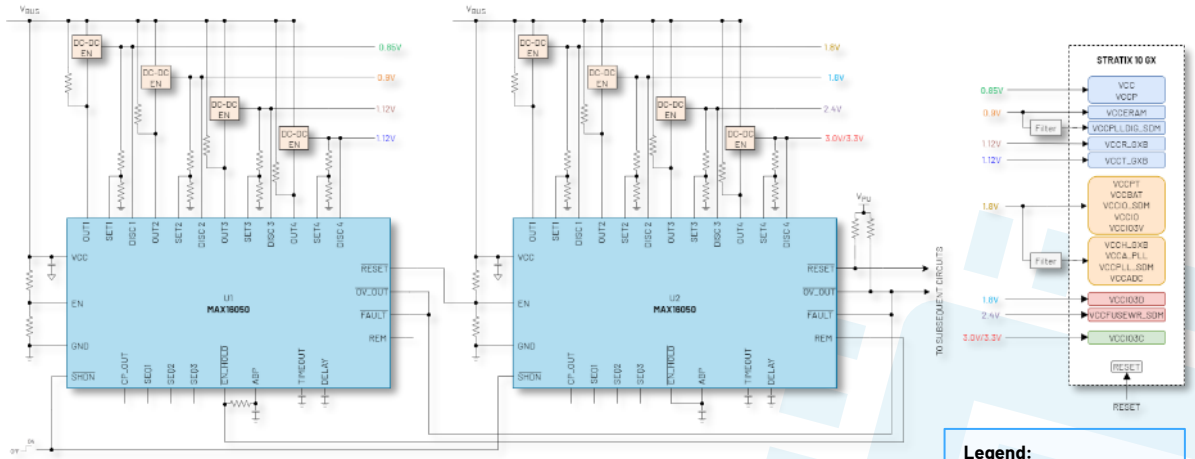
Number of Supplies Monitored	Part Number	Operating Vrange	Threshold Accuracy	Sequence	Programming Method	Package
1: cascadable	MAX16895	1.5 to 5.5V	1%	Up	R's, C's	6 uDFN
1: cascadable	MAX16052, MAX16053	2.25 to 28V	1.8%	Up	R's, C's	6 SOT23
2: cascadable	MAX6819, MAX6820	0.9 to 5.5V	2.6%	Up	R's, C's	6 SOT23
2	MAX16041	2.2 to 28V	2.7% and 1.5%	Up	R's, C's	16 TQFN
3	MAX16042					20 TQFN
4	MAX16043					24 TQFN
4: cascadable	MAX16165, MAX16166	2.7 to 16V	0.80%	Up, Reverse-Power Down	R's, C's	20 WLP, 20L TQFN
	MAX16050	2.7 to 16V	1.5%	Up, Reverse-Power Down	R's, C's	28 TQFN
5: cascadable	MAX16051					
6: cascadable	LTC2937	4.5 to 16.5V	<1.5%	Programmable	I2C, SMBus	28 QFN
8	ADM1168	3 to 16V	<1%	Programmable	SMBus	32 LQFP
8	ADM1169	3 to 16V	<1%	Programmable	SMBus	32 LQFP, 40 LFCSP
10: cascadable (max of 4)	ADM1260	3 to 16V	<1%	Programmable	SMBus	40 LFCSP
12: cascadable	ADM1166	3 to 16V	<1%	Programmable	SMBus	40 LFCSP, 48 TQFP
17: cascadable	ADM1266	3 to 15V	<1%	Programmable	PMBus	64 LFCSP



Power Supply Sequencing for Intel® Arria® 10 GX
with Transceiver Data Rate <= 11.3 Gbps for Chip-to-Chip Applications

Legend:
Power Group 1 - Blue
Power Group 2 – Orange
Power Group 3 – Red

MAX16050/MAX16051: Voltage Monitors/Sequencer Circuits with Reverse-Sequencing Capability



Power Supply Sequencing for Intel® Stratix® 10 GX
(only for the HF35 Package) with 15 Gbps < Transceiver Data Rate <= 28.3 Gbps

Legend:
Power Group 1 - Blue
Power Group 2 – Orange
Power Group 3 – Red
Power Group 4 - Green

Power Supply Sequencing with **MAX16050** using daisy chaining capability